Simple and Reliable Digital Electronics for Beam Monitoring and Control

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Modern digital electronics chips available on the market have reached incredible levels of performance. They enable highly advanced monitoring and control of accelerated beams, with bunch-by-bunch resolution and even beyond. However, this **performance comes at a cost**: increasing device capabilities also leads to greater complexity, making these technologies less accessible to beginners and often increasing development time.

On the other hand, many applications do not require state-of-the-art performance. In this contribution, we present a project that aims to remain relatively simple while providing intermediate levels of signal-processing and computational performance without compromising reliability.

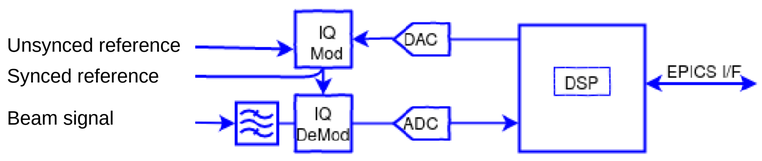
This project uses an FPGA to achieve precise control at the clock-cycle level. The purpose is to make a beam phase-lock loop, which would then provide a RF signal in phase with the beam for other diagnostics devices. Other applications based on the same hardware platform could later be realised, whether for feedback systems or simply for acquisition and monitoring.

We want to favour open-source components and solutions whenever possible, in order to facilitate reuse, adaptation, and long-term maintainability while reducing dependence on proprietary solutions.

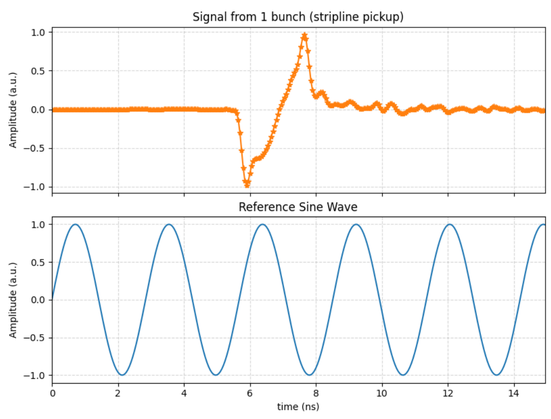
Beam Phase-lock loop:

The purpose of this project is to make a beam phase-lock loop, which would then provide a RF signal in phase with the beam for other diagnostics devices [1].

This is a similar project as done at DLS [2]:



Below is the signal from a (not so good) stripline pick-up. A reference signal is shown below.



We want to measure the phase of the bunch signal with respect to the reference signal.

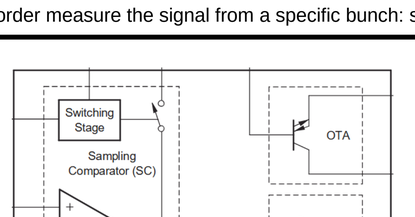
→ challenging when only one bunch is present in the storage ring

An FPGA will be used in order to easilly achieve precise sampling timing and fast feedback loop (1 us loop is the target).

The phase is measured by IQ demodulation of the beam signal. Precise sampling (~ ns) of the IQ values is necessary for few bunches filling modes.

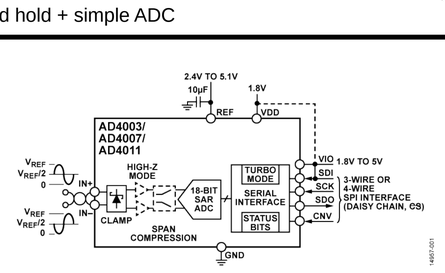
This is achieved with the following ICs:

In order measure the signal from a specific bunch: sample and hold + simple ADC



TI OPA615 Sample and Hold
(700 MHz bandwidth)

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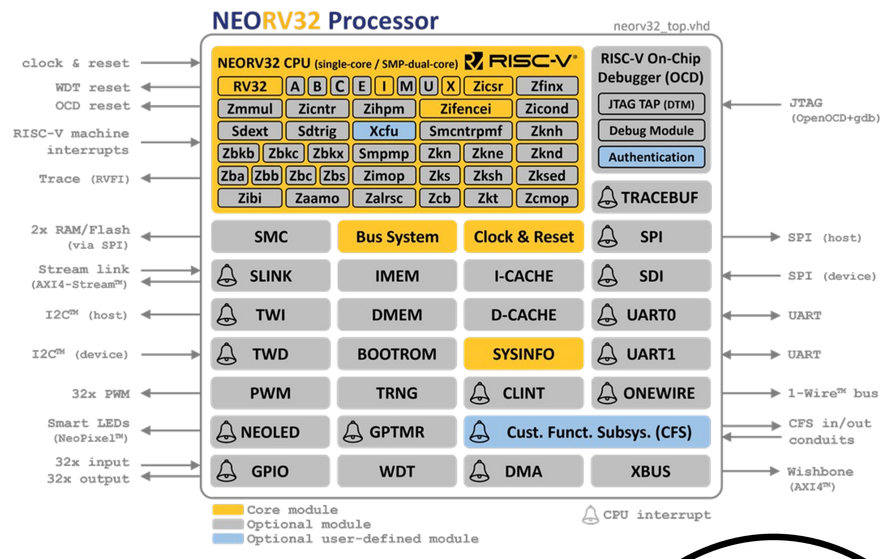


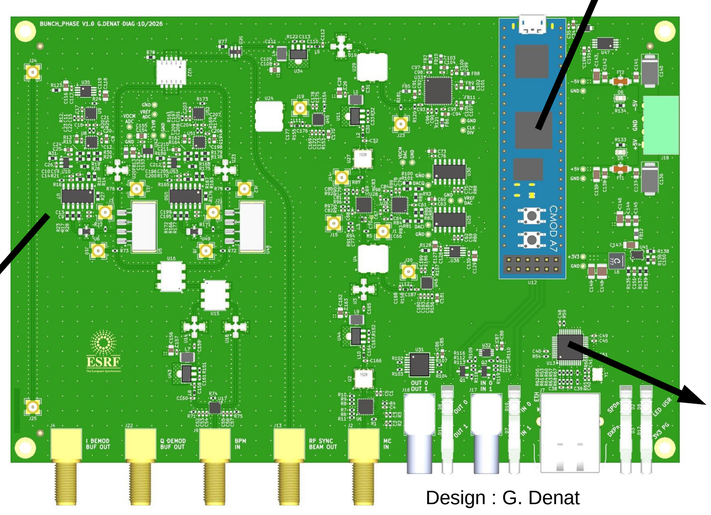
AD4003: an ADC with simple SPI interface

Control logic:

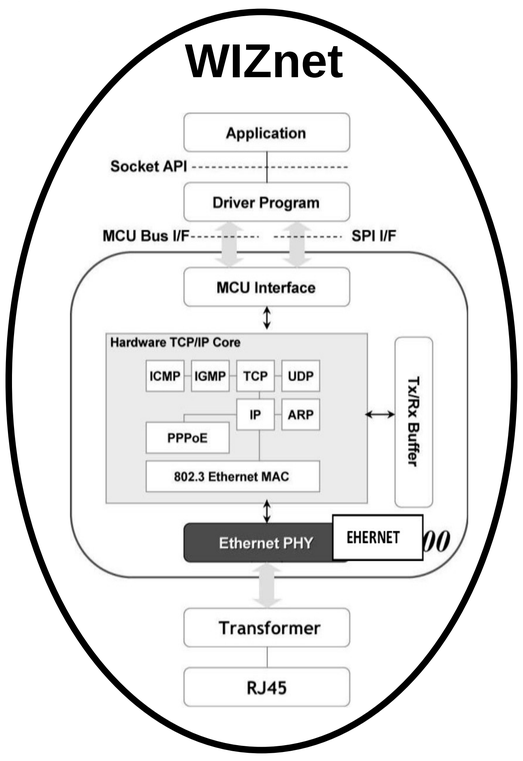
A key requirement for this project was the integration in the control system through TCP/IP, although the required bandwidth and interface speed is very low.

The control logic will be performed with a RISC-V soft-core embedded in the FPGA (neorv32, open source project). Communication with the control system is achieved with a Ethernet chip from WIZnet integrating a (simple) TCP/IP stack.





Design : G. Denat



Tango server (software layer):

A generic Tango server called ModbusComposer will be used to interface with the soft-core.

Job opportunity at the ESRF (LLRF)

ESRF is looking for an **Electronics Engineer** (3-year contract) to contribute to the COLD Project for: 1) Installation and commissioning of the **Digital Low-Level RF (LLRF)**, 2) Develop and execute detailed test and characterisation of amplitude and phase stability, noise and disturbance rejection, breakdown rates 3) Contribute to **automated RF testing, measurement, and power conditioning** of accelerating structures, RF photo-guns and deflecting cavities. Check ESRF website for more information!

[1] Single bunch phase measurement, B. Roche, **DEELS 2026**
[2] Tracking Frequency Reference Phase Changes at Point of use based on BPM Measurements, A. Tipper et al, **IBIC 2020**

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