Optimizing an RFSoC LLRF Controller for a Short-Pulse, Low-PRF System: Calibration, Measurements, Predictions

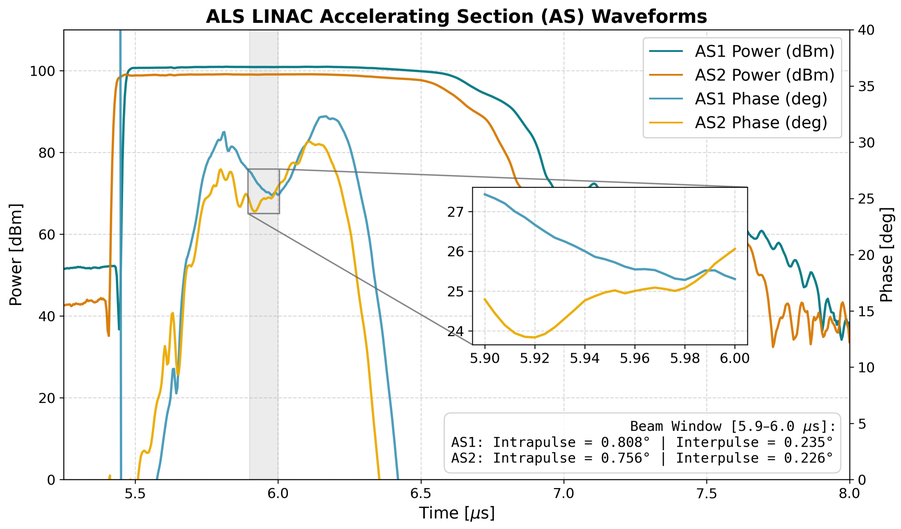
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ALS LINAC System Context

System Overview & Requirements: The Advanced Light Source (ALS) LINAC operates at 3 GHz RF with 0.7 Hz PRF and 1.2 μs pulse duration, limiting closed loop control. Existing high-power RF tuning requires open-loop amplitude control.

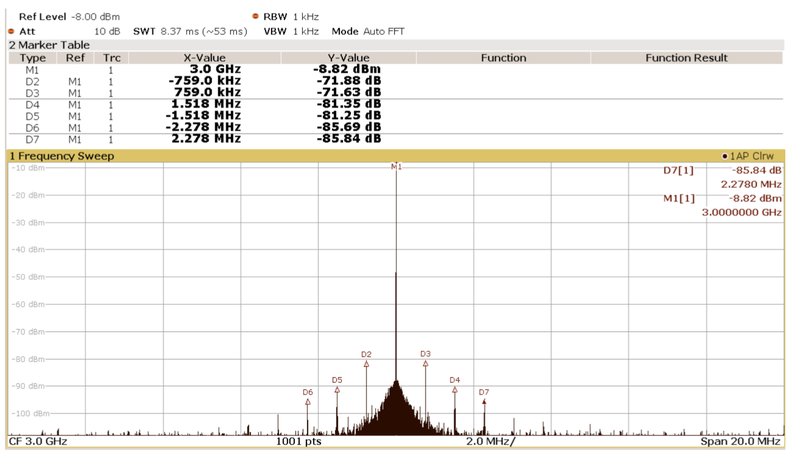
Control Dynamics & Limits:

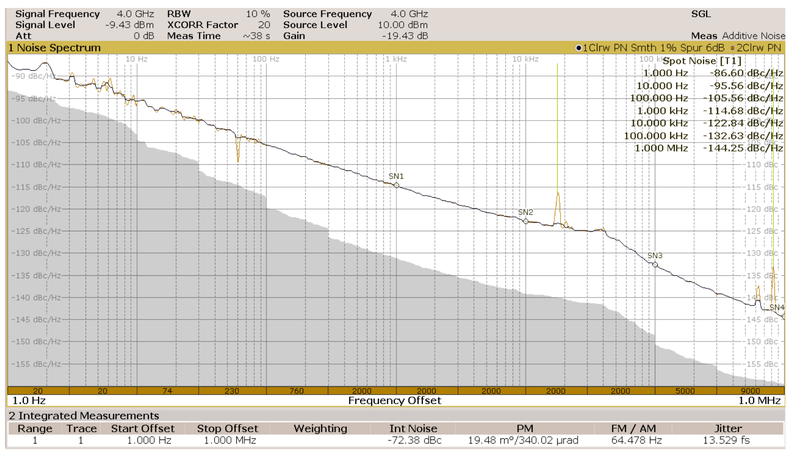
- **PI Bandwidth Limit:** Total loop latency ($\tau_{\text{total}} = 450$ ns, $\tau_{\text{rfsoc}} = 290$ ns) limits BW to 100 kHz. Settling time (4.8 - 6.4 μs) exceeds 1.2μs pulse length.
- **AFF Nyquist Constraint:** At 0.7 Hz PRF, Q-filter $\text{BW}_Q < 0.35$ Hz limits Adaptive Feed Forward feature size to DC corrections.
- **Relevant Noise:** For this DC-interpulse control, Tx noise determines LLRF added error. Rx noise determines RFSoC diagnostic capability.



DAC Performance & LLRF Predictions

DAC Output Spectrum & Phase Noise: The DAC spectrum exhibits 759 kHz modulating spurs. At 4 GHz, DAC additive phase noise is 13.5 fs [1Hz, 1 MHz] in isolation.



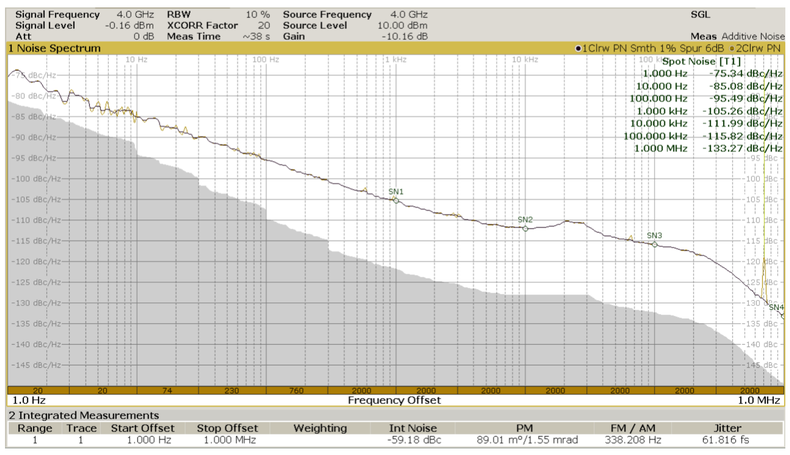


Parameter Source	Phase Error	Timing Jitter
DAC + Sampling Clock Phase Noise	0.046° RMS	43 fs RMS
Tx Modulating Spurs (759 kHz)	0.020° RMS	18 fs RMS
Open-Loop Phase Error (RSS)	**0.050° RMS**	**46 fs RMS**

CLK104A Sampling Clock Generation

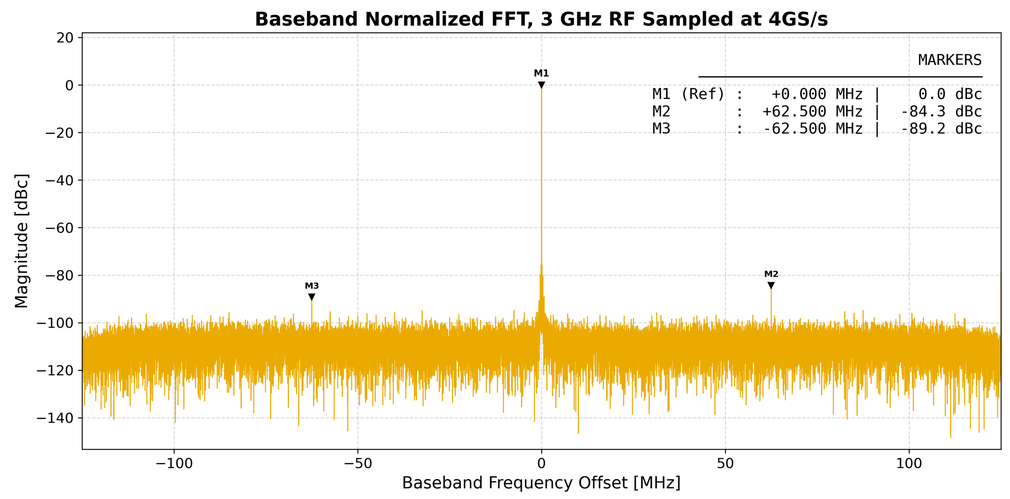
CLK104A: Modified Xilinx Hardware

Modified to bypass 'jitter cleaner': 61.8fs RMS [1Hz, 1MHz]

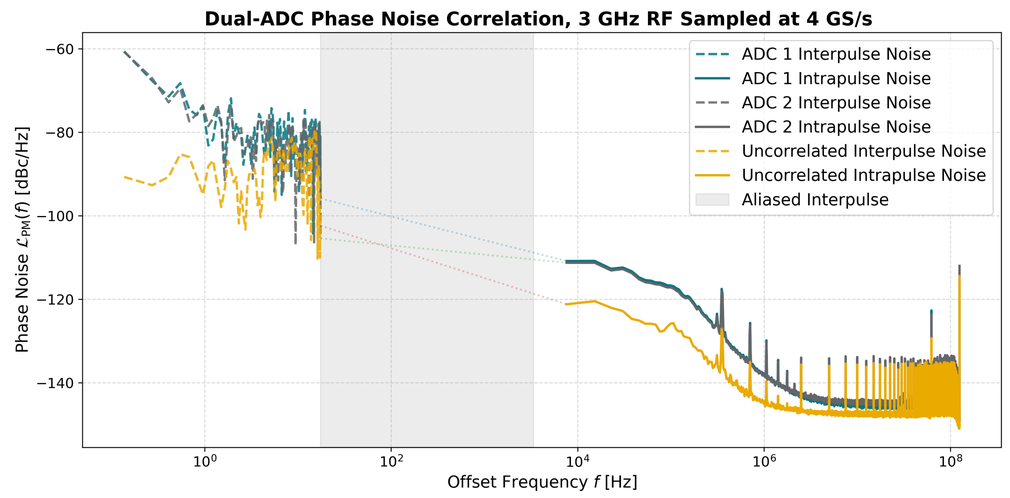


ADC Interleaving Calibration & Noise Measurement

1. Interleaving Spur Calibration: Interleaved sub-ADCs generate spurs at $k \cdot F_s/N$. Zero-IF folding at $f_{\text{RF}} = \frac{A \cdot f_s}{2M}$ is resolved by offset NCO calibration, suppressing interleaving spurs > 90 dBc (1.7fs).



2. Dual-ADC Uncorrelated Noise Characterization:



Parameter	Interpulse	Intrapulse	Total
Spectral Limits	0.1Hz, 3.4kHz	7.6kHz, 125MHz	—
ADC 1 / ADC 2 Noise	44/41 fs	73/76 fs	85/86 fs
Correlation (ρ_{12})	+94%	+67%	—
ADC Noise (σ_{uncorr})	**10 fs**	**43 fs**	**44 fs**
ADC + CLK104A	**43 fs**	**75 fs**	**86 fs**

Additive Jitter Component Summary

Component	Additive Jitter	Eval. Freq
CLK104A	62 fs RMS	4 GHz
DAC + CLK104A	61 fs RMS	4 GHz
DAC	13 fs RMS	4 GHz
ADC + CLK104A	86 fs RMS	3 GHz

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